**DAILY ASSESSMENT REPORT**

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| **Date:** | **04/06/2020** | **Name:** | **Yashaswini R** |
| **Subject:** | **Digital Design Using HDL** | **USN:** | **4AL17EC098** |
| **Topic:** | **Hardware modelling using Verilog. FPGA and ASIC Interview questions** | **Semester & Section:** | **6th B** |
| **GitHub Repository:** | **Yashaswini** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| Report VLSI Design   * Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. * The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in large scale integration technologies and system design applications. * With the advent of very large-scale integration (VLSI) designs, the number of applications of integrated circuits (ICs) in high-performance computing, controls, telecommunications, image and video processing, and consumer electronics has been rising at a very fast pace. * The current cutting-edge technologies such as high resolution and low bit-rate video and cellular communications provide the end-users a marvelous amount of applications, processing power and portability. * This trend is expected to grow rapidly, with very important implications on VLSI design and systems design.  1. Physical design:  * In this step the circuit representation (or netlist) is converted into a geometric representation. As stated earlier, this geometric representation of a circuit is called a layout. Layout is created by converting each logic component (cells, macros, gates, transistors) into a geometric representation (specific shapes in multiple layers), which perform the intended logic function of the corresponding component. Connections between different components are also expressed as geometric patterns typically lines in multiple layers.  1. Fabrication:  * After layout and verification, the design is ready for fabrication. Since layout data is typically sent to fabrication on a tape, the event of release of data is called Tape Out. Layout data is converted (or fractured) into photo-lithographic masks, one for each layer. Masks identify spaces on the wafer, where certain materials need to be deposited, diffused or even removed. Silicon crystals are grown and sliced to produce wafers. Extremely small dimensions of VLSI devices require that the wafers be polished to near perfection. The fabrication process consists of several steps involving deposition, and diffusion of various materials on the wafer. During each step one mask is used. Several dozen masks may be used to complete the fabrication process.  1. Packaging, Testing and Debugging:  * Finally, the wafer is fabricated and diced into individual chips in a fabrication facility. Each chip is then packaged and tested to ensure that it meets all the design specifications and that it functions properly. Chips used in Printed Circuit Boards (PCBs) are packaged in Dual In-line Package (DIP), Pin Grid Array (PGA), Ball Grid Array (BGA), and Quad Flat Package (QFP). Chips used in Multi-Chip Modules (MCM) are not packaged, since MCMs use bare or naked chips.  1. Moore's Law  * Moore's Law refers to Moore's perception that the number of transistors on a microchip doubles every two years, though the cost of computers is halved. Moore's Law states that we can expect the speed and capability of our computers to increase every couple of years, and we will pay less for them.   Task (DAY - 4)  Implement a simple T Flipflop and test the module using a compiler  Verilog Code:  module t\_ff (t,q,clk); input t,clk;  output reg q = 0;  always  @(posedgeclk)  begin  if (t==1)  begin  q=~q; end  else  begin  q=q; end  end  endmodule |

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| **Date:** | **04/06/2020** | **Name:** | **Yashaswini R** |
| **Course:** | **The Python Mega Course: Build 10**  **Real World Applications** | **USN:** | **4AL17EC098** |
| **Topic:** | **1] Application 8: Build a Web-based Financial Graph** | **Semester & Section:** | **6th B** |
| **GitHub Repository:** | **Yashaswini** |  |  |

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| AFTERNOON SESSION |
| Images of session    Report:  Application 8: Build a Web-based Financial Graph   * Python script to plot stock market data using bokeh library and deploy the bokeh plot to a live website. * A ticker symbol or stock symbol is an abbreviation used to uniquely identify publicly traded shares of a particular stock on a particular stock market. * A stock symbol may consist of letters, numbers or a combination of both. "Ticker symbol" refers to the symbols that were printed on the ticker tape of a ticker tape machine. * Some of the examples are:   + NYSE (New York Stock Exchange) uses the ticker symbol with 3 letters or few – such   as ‘NYT’ for the New York Times Co. or ‘T’ for AT&T.   * + Symbols with 4 or more letters generally denote securities traded on the American stock exchange and NASDAQ.   + Those ending in ‘X’ indicate mutual funds.   + There are also certain symbols that denote specific status or type ofsecurity say, tickers ending in ‘Q’ indicate issuers which are under bankruptcy and letter ‘Y’ denotes security is an ADR. * Some of the functions used under bokeh library:   + It is possible to ask Bokeh to return the individual components of a standalone document for individual embedding using the components () function under bokeh.embed module. This function returns a <script> that contains the data for your plot, together with an accompanying <div> tag that the plot view is loaded into. These tags can be used in HTML documents however you like.   + The resources module provides the Resources class for easily configuring how BokehJS code and CSS resources should be located, loaded, and embedded in Bokeh documents.   + Additionally, functions for retrieving Sub resource Integrity hashes for Bokeh JavaScript files are provided here   + Content delivery network (CDN): Load minified BokehJS from CDN. |